A MISMATCH MODEL OF TEMPERATURE DEPENDENT AND DEVICE DIMENSION ON THE THRESHOLD VOLTAGE OF MOSFET IN VLSI

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Abstract

The CMOS fabrication technology requires both n-channel (NMOS) and p-channel (PMOS) transistors be built on the same substrate. To ensure the reliability of the circuit performance over the temperature range, the circuits must be designed accommodate the basic variations parameters as a function of parameter. In this paper, The temperature dependence of the MOSFET parameters as well as the small dimension effects on the threshold voltage over the temperature range of 27- 125 degree Celsius are discussed and the simplicity macro mismatch model are presented. The results show that the threshold voltage temperature coefficient (TCV) of testing devices is increased as the channel width decreased. The measured threshold voltage compared with predicted mismatch model was low level error.

Keywords: CMOS, NMOS, PMOS, TCV

Introduction

When the devices are scale down to submicron. The relationship between the threshold voltage and the substrate bias deviate from the first order square root dependence as the device dimensions are scale down too. This is mainly because the built-in potential depends logarithmically on the substrate doping which is scaled up proportionally with the dimensions. This feature is modeled by decoupling the effect of channel length, channel width and a static feedback. Each of features is enable by specifying the parameters XJ, DELTA and ETA respectively. The short channel effect, the decrease of V_{TH} as the channel length is scaled down by Dang's[1]. The narrow channel effect, the increase of V_{TH} as the channel width is scaled down is model by taking into account the extra bulk charge at the edge of the channel such as the existence of field implant and non-planarity due to the LOCOS process. The parameter DELTA is introduced. The static feedback effect can be explained as a Drain Induced Barrier (DIBL) which is linearly proportional to V_{DS}. The threshold voltage in Level 3 model [2] which sums up the above feature is given below

$$V_{TH} = V_{TO} \mp \gamma\sqrt{\Phi_S} \pm \gamma F_S \sqrt{\Phi_S + |V_{BS}|} \pm F_N \left(\Phi_S + |V_{BS}|\right) - F_D V_{DS} \quad (1)$$

$$V_{TO} = V_{FB} + \Phi_S + \gamma\sqrt{\Phi_S} \quad (2)$$

$$\Phi_S = 2\phi_F = \frac{2kT}{q}\ln\left(\frac{N_{sub}}{n_i}\right) \quad (3)$$

$$\gamma = \frac{\sqrt{2q\varepsilon_{si}N_{sub}}}{C_{ox}} \quad (4)$$

where V_{TO} is a zero bias threshold voltage of a big MOSFET at zero substrate bias. V_{FB} is a flate band voltage. Φ_S is a surface potential. $Nsub$ is a substrate concentration. n_i is an intrinsic concentration = 1.1×10^{10} cm^{-3}. γ is a bulk threshold parameter. C_{ox} is an oxide thickness per unit area. ε_{si} is a permittivity of silicon dioxide.

For big MOSFET (large W, large L) , $F_S \rightarrow 1$, $F_N \rightarrow 0$. The equation of the narrow channel width at zero substrate bias voltage is simplified as

$$V_{TH} = V_{TO} \pm F_N(\Phi_S) \quad (5)$$

Similarly, the equation of the short channel width at zero substrate bias voltage and include drain bias is simplified as:

$$V_{TH} = V_{TO} \mp \gamma\sqrt{\Phi_S} \pm \gamma F_S \sqrt{\Phi_S + |V_{BS}|} - F_D V_{DS} \quad (6)$$

Where the upper cased Δ is referred the equation of NMOS; where as, the lower cased ∇ is referred the equation of PMOS respectively. Parameter F_N is the correction factor of a narrow channel [2] is simplified as below

$$F_N = DELTA\frac{\pi\varepsilon_{si}}{2C_{ox}W_{eff}} \quad (7)$$

The electrical characteristics of MOSFETs normally are strong dependence on the operating temperature. One of the main parameter is the low field mobility degradation decreased with temperature also the Φ_S and V_{FB} which decreased with temperature. The following temperature model of V_{TH} at zero substrate bias is used[3],[4],[5]

$$V_{TH}(T) = V_{TH}(T_{ref}) + TCV(T - T_{ref}) \quad (8)$$

Where $V_{TH}(T)$ is a threshold voltage depended on operating temperature, T_{ref} is the reference temperature at which parameters are extracted (27^0C), TCV is the threshold voltage temperature coefficient.

The new modify simplicity equation includes narrow width dimension structure and temperature dependent affect on threshold voltage of MOSFETs can be defined as

$$V_{TH,N}(T) = [V_{TH,B}(T_{ref}) + TCV_B(T - T_{ref})] + F_N \Phi_S(T) \quad (9)$$

$$F_N \Phi_S(T) = F_N \Phi_S(T_{ref}) + TCV_{FN}(T - T_{ref})\Phi_S(T - T_{ref}) \quad (10)$$

In simplicity way, it can be used in the following equation

$$V_{TH,N}(T) = V_{TH,N}(T_{ref}) + TCV_N(T - T_{ref}) \quad (11)$$

Where the subscript B and N are referred big channel width dimension and narrow channel width dimension of MOSFETs, the $TCVF_N$ is the threshold voltage temperature coefficient of The narrow channel width of MOSFETs. Where V_{TH}(T) is a threshold voltage depended on operating temperature, T_{ref} is the reference temperature at which parameters are extracted (27^0C), TCV is the threshold voltage temperature coefficient, UTE is the temperature effect on the low drain bias mobility. In this paper, The temperature dependence of the MOSFET parameters as well as the small dimension effects on the threshold voltage over the temperature range of 27- 125 degree Celsius are discussed and the new simplicity mismatch model are presented.

Methodology

The devices are made in the 0.8 um CMOS twin well CMOS technology. Twin well processes is used for NMOS and PMOS independently.The processes were done on 6 inches wafer <100> p-type silicon wafers with resistivity of 20 ohm-cm. The process fabrication included 8 lithography steps for front end of line (FEOL) and 5 lithography steps for back end of line (BEOL). The N-well and the P-well were fabricated by phosphorus with dose in order of 10^{12} cm^{-2} and boron implantation with dose in order of 10^{11} cm^{-2}, respectively. For LOCOS isolation, the field oxide thickness was 650 nm. The operation voltage should be more than 15 V because of this designed field oxide thickness. The N-field implantation beneath the field oxide was implanted for increasing the field oxide threshold voltage in order of V_{DS} + 10 V. The bird's break encroachment must be controlled because it affects the source/drain formation. Besides this effect, the bird's beak encroachment into the active area must be determined in order to know the minimum designed gate width which has an enough active area will be formed. A 15 nm gate oxide was grown in a thermal furnace at 900°C in dry ambience. A 350 nm polysilicon with phosphorus implantation was fabricated for gate electrode. A boron ion implantation for threshold voltages adjustment in a channel was implemented in order to match the threshold voltage of the NMOS and PMOS device. As a result, a surface channel and a buried channel were formed in NMOS and PMOS respectively. Low energy implants are required to form shallow junctions self-aligned to the poly gate. Phosphorus and BF_2 implants formed the lightly doped drain (LDD) of NMOS and PMOS structure. To reduce the hot carrier, phosphorus with 6×10^{13} cm^{-2} and boron with 1×10^{13} cm^{-2} is implemented to form the lightly doped drain (LDD) of NMOS and PMOS structure Oxide sidewall spacers 250 nm of thickness were used as an implant mask for the source/drain region self-aligned to the shallow LDD. As and BF_2 are implemented to produce source/drain to achieve 54 Ω/sq for n^+ and 65 Ω/sq for p^+ source/drain. From simulation results, the S/D junction depth was 0.3 and 0.5 μm for NMOS and PMOS and the effective channel length was approximately 0.6 μm of both MOSFET also The measurement system is consists of probe station Cascade Microtech M150 model, Semiconductor Device analyser

B1500A and ERS Aiecool SP72 model. All I-V measurements were performed on NMOS

and PMOS devices with different dimensions (W/L= 20/20, 1.2/20, 2.4/20, 4.8/20, 20/0.8, 20/1.0, 20/1.2, 20/1.6, 20/3.0) to obtain a wide overview of device operational characteristics and meet the devices model. I_{DS}-V_{GS} measurements were done in both devices the linear mode ($|V_{DS}|$= 100 mV) and in the saturation mode ($|V_{DS}|$=5 V). The threshold voltage measurement has been done on a transistor array of different size. The threshold voltage measurement method is the linear extrapolation methodology as shown in Figure1. The scalable device of testing devices is illustrated in Figure 2.

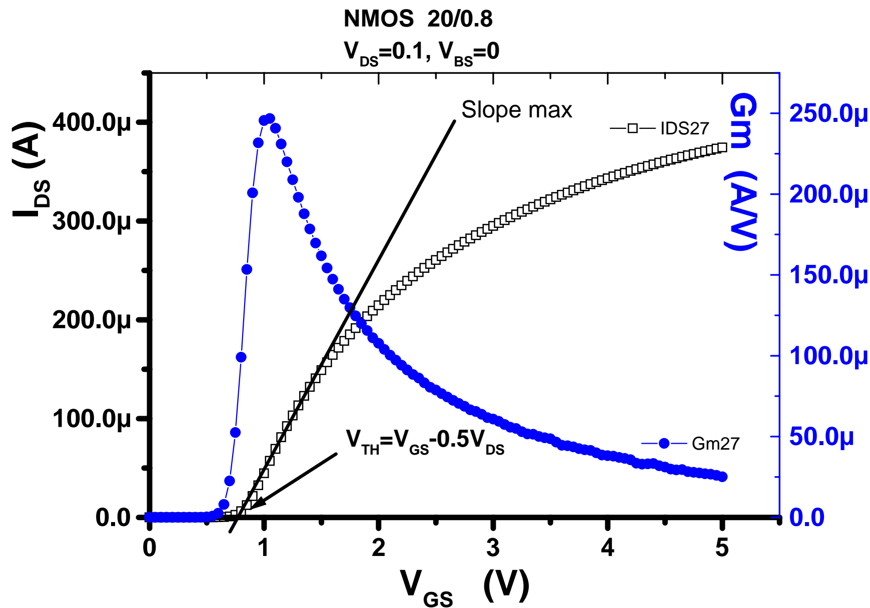

Figure 1 The threshold voltage measurement method of NMOS

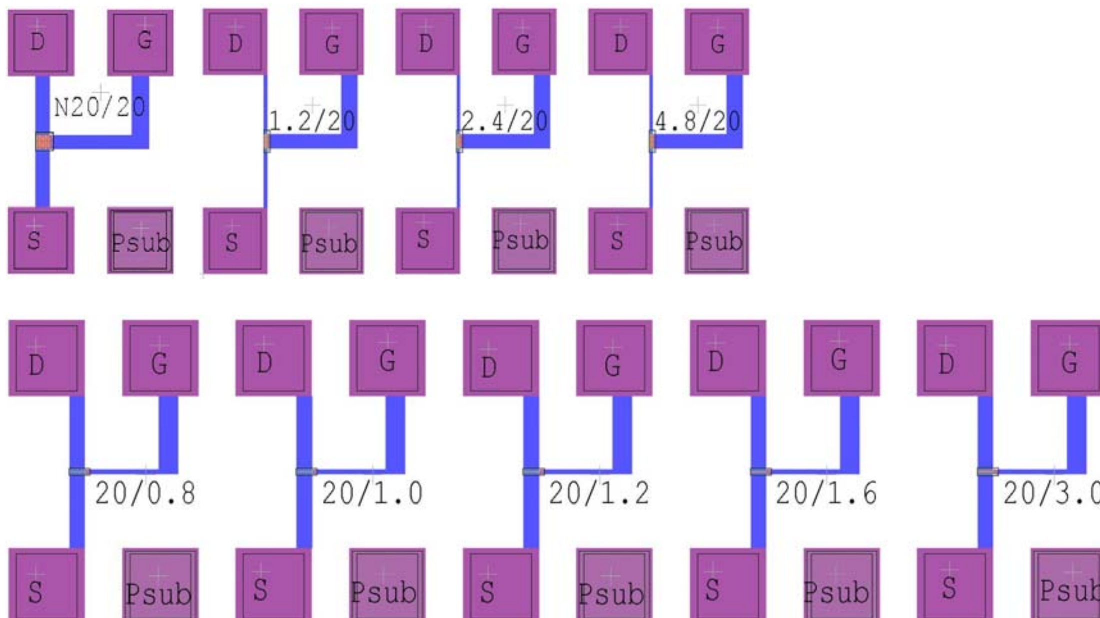

Figure 2 Illustration of the scalable device test structure at various W/L=20/20, 1.2/20, 2.4/20, 4.8/20, 20/0.8, 20/1.0, 20/1.2, 20/1.3 and 20/3.0 (µm/µm)

Results

The electrical parameters of both MOSFETs are illustrated in Table 1. At room temperature, the threshold voltage was extracted from the linear extrapolation methodology as shown in Figure 3. The extracted thresholds voltage at zero substrate bias voltage was 0.77 V and -0.9 V for NMOS and PMOS respectively. The DIBL effect is observed by a shifted of threshold voltage as a function of drain voltage. The threshold voltage measurement for testing device was performed by measuring a set of I_{DS}-V_{GS} with increasing V_{DS} value as a parameter. The gate voltage which the drain current of 0.1µA/µm is claimed the threshold voltage. The measured DIBL is 15 mV/V and 25 mV/V of NMOS and PMOS respectively. The total channel length reduction from drawn

Table 1 The electrical parameters of NMOS and PMOS at 27 and 125 degree calculus

W	L	27°C		125°C	
		V_{TH} (V) NMOS	V_{TH} (V) PMOS	V_{TH} (V) NMOS	V_{TH} (V) PMOS
20	20	0.77	-0.96	0.65	-0.79
20	0.8	0.77	-0.90	0.65	-0.77
4.8	20	0.81	-0.98	0.68	-0.81
2.4	20	0.85	-1.0	0.72	-0.84
1.2	20	1.4	-1.1	1.26	-0.94
3.6	0.8	0.79	-0.90	0.69	-0.73
2.4	0.8	0.89	-0.91	0.76	-0.74
1.2	0.8	0.93	-0.96	0.84	-0.80

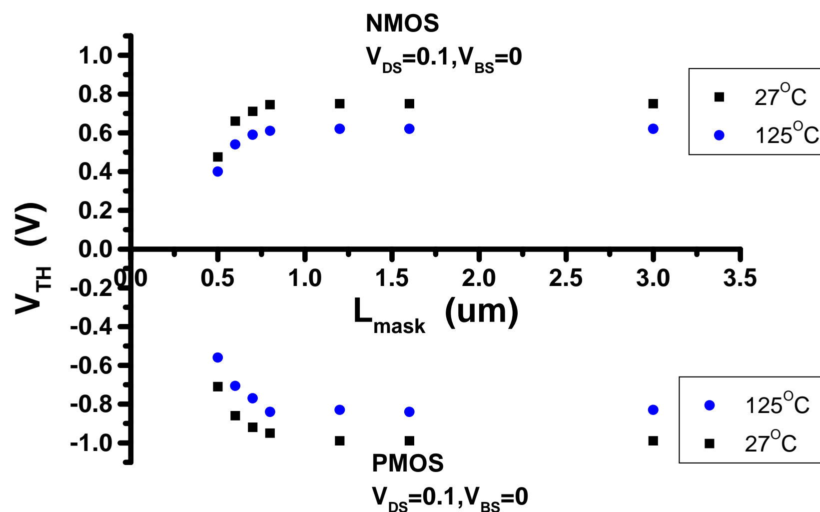

Figure 3 Measured V_{TH} versus L_{mask} of NMOS and PMOS at different temperature

The combination effects of temperature dependence and channel width reduction is still reflected in the lowering of threshold voltage of both MOSFETs. The significant parameters of narrow channel affect and the temperature dependence on threshold voltage are listed in Table 2.

Table 2 Electrical parameters of NMOS and PMOS (continue)

Parameter	NMOS	PMOS	Unit	Remark
TCV	-1.2	+1.4	mV/°C	W/L=20/0.8
TCV_N	-1.45	+1.6	mV/°C	W/L=1.2/20
FN@27	2.19×10^{-3}	7.99×10^{-4}		W/L=20/0.8
$TCVF_N$	6.0×10^{-6}	1.18×10^{-5}		W/L=20/0.8
FN@27	2.08×10^{-1}	7.59×10^{-2}		W/L=1.2/0.8
$TCVF_N$	5.78×10^{-4}	7.51×10^{-4}		W/L=1.2/0.8

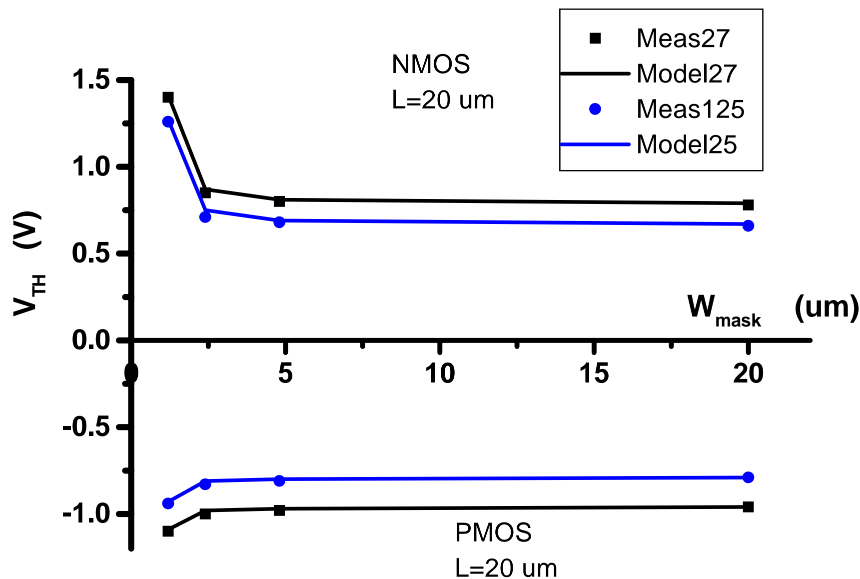

Figure 4 Measured versus predicted mismatch model of V_{TH} for W-array of NMOS and PMOS

Discussion and Conclusion

The results show that the TCV of PMOS is stronger than NMOS not only a large dimension but also a small dimension. The channel width affects on threshold of both devices increase as the temperature increase and strongly affect on NMOS more than PMOS. Similarly, the same results for the correction factor of a narrow channel. The measured threshold voltage compared with predicted mismatch model was low level error. The process parameters for instant Xj, Tox Nch, Nsub, poly silicon gate type and isolation technique are key parameter also. The results provide the data for process engineer and circuit designer in the next fabrications.

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References

1. L,M.Dang, A simple Current Model for Short Channel IGFET and its Application to Circuit Simulation, IEEE J. Solid State Circuit,Vol.Sc- 4, No.2, pp356-367,Apr (1979).
2. Anucha Ruangphanit, Rangson Muanghlua, Nopphon Phongphanchanthra, Amporn Poyai, "The Parameters Mismatch Model of Threshold Voltage For The Narrow and Short Channel MOSFET", The 10th Annual National Symposium on Computational Science and Engineering (ANSCSE10), 22-24 March 2006, Chiangmai, pp. 62-67.
3. Wang, R. DeMassa, T.A. and Jelsma, L.F. 1971. Threshold Voltage Variations with Temperature in MOS Transistor. IEEE Trans. Electron Devices. 18: 386-388.
4. Shoucair, F. Hwang, W. and Jain, P. 1984. Electrical Characteristics of Large Scale Integration (LSI) MOSFETs at Very High Temperatures. Microelectronics and Reliability, 24: part I 465-485 part II 487-510.